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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/492,789	01/28/2000	Takakazu Yano	01165.0770	1372

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EXAMINER
JORGENSEN, LELAND R

ART UNIT	PAPER NUMBER
2675	9

DATE MAILED: 10/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PRS

Office Action Summary	Application No.	Applicant(s)	
	09/492,789	YANO ET AL.	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. In view of applicant's July 29, 2002 amendment, the objection to the specification and abstract is withdrawn.

Drawings

2. In view of applicant's July 29, 2002 proposed drawing changes, the objection to the drawings is withdrawn.

Claim Rejections - 35 USC § 112

3. In view of applicant's July 29, 2002 amendment and remarks, the 35 U.S.C. 112 rejections are withdrawn.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1 (amended), 7 – 10, and 18 (new) are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al., USPN 5,663,743, in view of Sakamoto et al., USPN 3,956,661 and of Suzuki et al., USPN 4,621,260.

Claim 1

Claim 1 (amended) describes a power supply circuit.

Scan Driver Power Circuit. Fujii teaches a scan power supply circuit to supply scan drive voltage to a scan driver for scanning a liquid crystal display. Fujii, col. 4, lines 1 – 3; col. 5, lines 22 – 24, 29 – 36; and figures 1 and 2.

Data Driver Power Circuit. Fujii teaches a data power supply circuit to supply data drive voltage to a data driver for sending display data to a liquid crystal display. Fujii, col. 4, lines 1 – 3; col. 5, lines 15 – 17, 29 – 36; and figures 1 and 2. The data driver power circuit comprises the following.

Input Power Supply. Fujii teaches input power supply V_{CC} serving as a universal power supply. Fujii, figure 1; col. 5, lines 29 – 36; and col. 6, lines 4 – 8. Sakamoto also shows an input power supply, V_{cc}. Sakamoto, figure 2.

Amplifying Element. Claim 1 describes an amplifying element with an input terminal connected to the input power supply, a control terminal, and an output terminal from which the data power driver power voltage is outputted. The specification gives an example of an amplifying device being a bipolar transistor with the collector being the input terminal, the base being the control terminal, and the emitter being the output terminal. Fujii shows a transistor Tr with a collector, base, and emitter. Fujii, figure 1; and col. 6, lines 4 - 12. Sakamoto also teaches an amplifying element, showing a transistor 1 with a collector, base, and emitter. Sakamoto, figure 2; col. 2, lines 22 – 33.

Current Limiting Resister. Claim 1 describes an electric current limiting resister having the first terminal connected to the input power supply and the second terminal connected to the control terminal of the amplifying element. Fujii shows a variable resister R1 that has a portion of the resistance between the first terminal from the input power supply and a second

terminal connected to the control terminal of the amplifying element. The variable resister controls the electric current supplied to the base. Fujii, figure 1; and col. 6, lines 4 – 11. Sakamoto also shows a resister R1 with a first terminal connected to the connected to the input power supply and the second terminal connected to the control terminal of the amplifying element. Sakamoto, figure 2; col. 2, lines 22 – 33. Although Sakamoto does not describe the resister as current limiting, it would be an inherent that a resister so placed in this circuit would be current limiting.

Plurality of Series-Connected Diodes. Claim 1 describers a diode group including a plurality of series-connected diodes wherein a cathode terminal of a first diode is connected to ground and an anode terminal of a last diode is connected to the control terminal of said amplifying element, and each other diode in the series having a cathode terminal connected to an anode terminal of the preceding diode.

Fujii does not teach the series-connected diodes.

Sakamoto teaches a plurality of series connected diodes having a cathode end connected to the control terminal and the anode end connected to ground. Although figure 2 shows the diode group having two diodes, Sakamoto's figure 1 and specifications make it clear that the number of diodes is variable. Sakamoto, figure 1; col. 2, lines 22 – 33.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the temperature compensation power source circuit of Sakamoto with the data drive power circuit of Fujii to create a temperature compensation data drive power circuit. Sakamoto invite such combination by teaching,

> The present invention relates to an improved D.C. power source for stabilizing an output voltage and/or current especially in integrated circuits (IC)

> and also for compensating for deviation or fluctuation in the current amplification factor h_{FE} or β of a transistor due to variation in the ambient temperature.
>
> Heretofore, in a transistor circuit for supplying constant output voltage, a power supply voltage was divided by a pair of bias resistors including an emitter resistor in a transistor circuit built in an integrated circuit block, and the divided voltage was supplied to a transistor or transistors also built in the integrated circuit blocks. However, in a prior D.C. power source the compensation for preventing the change of the output voltage due to temperature change was not enough because the values of the resistances in the IC blocks were considerably varied by discrepancies among resistors as well as temperature variations, and it was very difficult to construct a transistor circuit in which an absolute value of the current flowing through a load was maintained constant.

Sakamoto et al., col. 1, lines 5 – 10. See also: Sakamoto, col. 1, lines 29 – 55, where Sakamoto explains the temperature compensation objects of its circuit.

Capacitor. Claim 1 adds a capacitor having a first terminal connected to said output terminal of the amplifying element, and a second terminal connected to ground.

Neither Fujii nor Sakamoto teach such capacitor.

Suzuki teaches as conventional a capacitor 12 having a first terminal connected to the output terminal of the amplifying element 2, and a second terminal connected to ground. Suzuki, col. 3, lines 40 – 60.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the capacitor as shown by Suzuki with the power supply circuit as taught by Fujii and Sakamoto to ground out high frequency noise at the output.

Claim 7

Seven Diodes. Claim 7 is dependant on claim 1 and adds that the number of diodes of the diode group is seven.

Sakamoto does not specify the number of diodes as seven.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use seven diodes in the diode group. Sakamoto invites one to vary the number of diode. After defining *m* as the number of diode between the control terminal and ground, Sakamoto states,

> As described above, whenever the dividing ration of the D.C. power supply voltage V_{CC} is desired, the first and second resisters R1 and R2 and values of *m* and *n* are in turn determined. Thus the effect of the change of the voltage drop between the base and emitter V_{BE} of the transistor 1 due to temperature change is completely avoided by inserting a predetermined number of diodes 6.

Sakamoto, col. 3, lines 17 – 24. For one of ordinary skill in the art at the time of the invention, it is an obvious design choice, as motivated by the above teachings of Sakamoto, to choose a certain number of diodes to set an appropriate voltage drop.

Claim 8

Silicon Diodes. Claim 8 is dependant on claim 1 and adds that the diodes of the diode group are silicon diodes.

Sakamoto does not specifically describe the diodes as silicon.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use silicon diodes for the diodes of the diode group. Silicon diodes are readily available and well know in the art, as admitted in applicant's specification, page 2, lines 11 – 12.

Claim 9

Resistance of Current Limiting Resister. Claim 9 is dependant on claim 1 and adds that the resistance of the current limiting resister is within a range of 40 kΩ to 50 kΩ.

Sakamoto does not specify the resistance of the current limiting resistor within a range of 40 kΩ to 50 kΩ.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a range. Sakamoto invites one to consider different resistances. Sakamoto, col. 3, lines 17 – 24. Sakamoto offers formulas to find such resistances. Sakamoto, col. 2, line 21 – col. 3, line 32. For one of ordinary skill in the art at the time of the invention, it is an obvious design choice, as motivated by the above teachings of Sakamoto, to choose a certain resistance to produce an appropriate current.

Claim 10

Bipolar Transistors. Claim 10 is dependant on claim 1 and adds that the amplifying elements are bipolar transistors. Sakamoto teaches a transistor. Sakamoto, figure 2, col. 2, lines 22 – 33. Although Sakamoto does not teach in the specifications that the transistors are bipolar, bipolar transistors would be inherent because the symbol of the transistor used in Sakamoto's figures are those typically used for bipolar transistors.

Claim 18

Claim 18 (new) is dependant on claim 1. Fujii teaches a voltage regulation function and a power supply function for the liquid crystal display. Fujii, col. 4, lines 1 – 3; col. 5, lines 15 – 24, 29 – 36; and figures 1 and 2. Sakamoto teaches a temperature compensation function. Sakamoto, col. 1, lines 5 – 10, 29 – 55. It is inherent that the data driver power circuit described by Fujii and Sakamoto would perform these functions at the same time.

6. Claims 11 - 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al., Fujii et al., and Suzuki et al., as applied to claim 1 above, and further in view of The Electrical Engineering Handbook, CRC Press, 1993.

Claim 11

Field Effect Transistors. Claim 11 is dependant on claim 1 and adds that the amplifying elements are field effect transistors. Sakamoto teaches a transistor. Sakamoto, figure 2, col. 2, lines 22 – 33. Fujii teaches MOS transistors. Fujii, figure 1; and col. 6, lines 12 – 14. A MOS transistor is a type of field effect transistor.

Sakamoto does not teach that the transistors are field effect transistors and Fujji uses the MOS transistors in a slightly different way in its circuit.

The Electrical Engineering Handbook teaches the use of field effect transistors. Handbook, p. 545.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use field-effect transistors for transistors in the data driver power circuit of Sakamoto. The Handbook teaches, "There are two basic forms of transistors, the *bipolar* family and the *field-effect* family, and both appears in ICs. They differ in their modes of operation but may be incorporated into circuits in quite similar ways." Handbook, p. 545. Field-effect transistors are readily available and easy to use.

Claim 12

MOS Transistors. Claim 12 is dependant on claim 1 and adds that the amplifying elements are MOS transistors. Sakamoto teaches a transistor. Sakamoto, figure 2, col. 2, lines 22 – 33. Fujii teaches MOS transistors. Fujii, figure 1; and col. 6, lines 12 – 14.

Sakamoto does not teach that the transistors are MOS transistors and Fujji uses the MOS transistors in a slightly different way in the circuit.

The Electrical Engineering Handbook teaches the use of MOS transistors. Handbook, p. 567 – 580.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use MOS transistors for transistors in the data driver power circuit of Sakamoto. The Handbook teaches that MOS transistors allow easy fabrication using lithographic processes, resulting in integrated circuits (ICs), with very small devices, very large device counts, and very high reliability at low cost. MOS transistors also allow manufacture of complex systems without expensive packaging or cooling requirements. Handbook, p. 568. A MOS transistor, often labeled a MOS-FET, is a type of field effect transistor.

7. Claims 2 - 4 and 14 - 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al., Fujii et al., and Suzuki et al., as applied to claim 1 above, and further in view of Nishioka, et al., USPN 6,121,943.

Claim 2

Claim 2 is dependant on claim 1 and adds details of the scan driver power circuit.

Input Power Supply. Claim 2 describes an input power supply serving as a universal power supply. Fujii teaches input power supply V_{CC} serving as a universal power supply. Fujii, figure 1; col. 5, lines 29 – 36; and col. 6, lines 4 – 8. Nishioka also teaches a power supply 80. Nishioka, figures 4 and 6, col. 5, lines 51 – 55.

Amplifying Element. Claim 2 describes an amplifying element with an input terminal connected to the input power supply, a control terminal, and an output terminal from which the data power driver power voltage is outputted.

Sakamoto does not teach an amplifying element. Fujii teaches an amplifying element for the data driver power supply with the input terminal connection to the input power supply and different amplifying elements for the scan driver power supply. The terminal connections for the amplifying element for the scan power supply, however, do not track the terminal connections of claim 2. Fujii, figure 1.

Nishioka teaches a amplifying element 81a with an input power supply, control terminal, and output terminal from which the data power driver voltage is outputted. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5.

Divider Circuit. Claim 2 describes a divider circuit between the input power supply and ground. The divider circuit sets an upper value of a voltage applied to the control terminal of the amplifying element of the scan driver power circuit.

Sakamoto and Fujii do not teach such divider circuit.

Nishioka teaches such divider circuit. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5. See discussion in claim 3 below.

Variable Resister. Claim 2 describes a variable resister having a resistance variation terminal connected to the control terminal of the amplifying element. The variable resistors allows the voltage at the output terminal to vary by changing the voltage at the control terminal.

Sakamoto does not teach a variable resister. Fujii teaches an variable resister for the data driver power supply with the input terminal connection to the input power supply and a different variable resister for the scan driver power supply. The terminal connections for the variable resister for the scan power supply, however, do not track the terminal connections of claim 2. Fujii, figure 1.

Nishioka teaches a variable resister 81b having a resistance variation terminal connected to the control terminal of the amplifying element. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the constant current control circuit of Nishioka to the display voltage supply circuit of Fujii and Sakamoto to create a scan driver power circuit. Nishioka points out that "It is an object of the present invention to solve the problems associated with the generation of heat and the rush current during the application of the scan signal while reducing the charging and discharging time." Nishioka, col. 1, lines 54 – 57. Nishioka teaches the advantage of its power circuit for scan driver. "Thus, the constant current control circuit 81 performs control to provide a constant current in response to the control signal at a high level input from the input terminal S1. Nishioka, col. 6, lines 2 – 5.

Claim 3

Claim 3 is dependant on claim 2 and adds that the divider circuit comprises the following.

Resister. Claim 3 describes a resister having a terminal connected to the input power supply. Nishoida teaches a resister 81c. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5.

Zener Diode. Claim 3 describes a Zener diode having a cathode connected to the resister and an anode to ground. Nishioka teaches a Zener diode 81d having a cathode connected to the resister and an anode to ground. Nishioka, figures 4 and 6 and col. 6, lines 19 – 21.

Claim 4

Variable Resistor Connected to Zener Diode. Claim 4 is dependant on claim 3 and adds that the terminal of the variable resistor is connected to the cathode of the Zener diode.

Nishioka teaches that the terminal of the variable resister 81b is connected to the Zener diode 81d. Nishioka, figures 4 and 6 and col. 6, lines 19 – 21.

Claim 14

Bipolar Transistors. Claim 14 is dependant on claim 2 and adds that the amplifying elements are bipolar transistors. Nishioka teaches the use of bipolar transistors in the scan driver and the data driver. Nishioka, col. 8, lines 44 – 48. See rejection of claim 10 which is hereby incorporated into the rejection of claim 14.

Claim 15

Field Effect Transistors. Claim 15 is dependant on claim 2 and adds that the amplifying elements are field effect transistors. Nishioka teaches the use of field effect transistors (FET). Nishioka, col. 5, line 59 – col. 6, line 5. See rejection of claim 11 which is hereby incorporated into the rejection of claim 15.

8. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al., Fujii et al., and Suzuki et al., as applied to claim 1 above, and further in view of Ikeda, USPN 6,236,394 B1.

Claim 5

Range of Voltage. Claim 5 is dependant on claim 1 and adds that the data drive voltage is within a range of voltage that is lower than the threshold voltage of a liquid crystal used in the liquid crystal display device by 20 percent of the threshold voltage to a voltage that is higher than the threshold voltage by 20 percent of the threshold voltage.

Sakamoto does not specify an actual voltage range although Sakamoto presents voltage equations for the data driver power supply circuit. Sakamoto, col. 2, line 21 – col. 3, line 32. Likewise, Fujii has an equation for the power consumption and shows a relationship between the scan drive power and the data drive power but again does not describe a range. Fujii, col. 6, lines 45 – 61; col. 7, line 13; and figure 4.

Ikeda, however, teaches a maximizing power consumption relationship between scan drive power (labeled the duty ratio) and data drive power (optimum boosting ratio) that invites one skilled in the art to discover the 20 percent range. Ikeda, col. 8, lines 1 – 38; and figures 5A and 5B.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the equations of Sakamoto and Fujii with the maximizing power consumption relationship of Ikeda to find the range described in claim 5. Sakamoto and Fujii invites one to find this range by presenting voltage equations. Ikeda teaches "The unnecessary power consumption can effectively be reduced since the boosting and deboosting ratio can be controlled according to the duty ratio." Ikeda, col. 2, lines 65 – 67. See also Ikeda, col. 1, lines 5 – 15, 26 – 30; and col. 2, lines 14 - 19.

Claim 6

Range of Voltage. Claim 6 is dependant on claim 1 and adds that the data drive voltage is within a range of 20 percent lower than a peak to peak voltage of a signal to 20 percent higher than a peak to peak of signal that is imputed to the data driver.

Sakamoto does not specify an actual voltage range although Sakamoto presents voltage equations for the data driver power supply circuit. Sakamoto, col. 2, line 21 – col. 3, line 32.

Likewise, Fujii has an equation for the power consumption and shows a relationship between the scan drive power and the data drive power but again does not describe a range. Fujii, col. 6, lines 45 – 61; col. 7, line 13; and figure 4.

Ikeda, however, teaches a maximizing power consumption relationship between scan drive power (labeled the duty ratio) and data drive power (optimum boosting ratio) that invites one skilled in the art to discover the 20 percent range. Ikeda, col. 8, lines 1 – 38; and figures 5A and 5B.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the equations of Sakamoto and Fujii with the maximizing power consumption relationship of Ikeda to find the range described in claim 5. Sakamoto and Fujii invites one to find this range by presenting voltage equations. Ikeda teaches "The unnecessary power consumption can effectively be reduced since the boosting and deboosting ratio can be controlled according to the duty ratio." Ikeda, col. 2, lines 65 – 67. See also Ikeda, col. 1, lines 5 – 15, 26 – 30; and col. 2, lines 14 - 19.

9. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al., Sakamoto et al., Suzuki et al., and Nishioka, et al. as applied to claim 2 above, and further in view of The Electrical Engineering Handbook.

Claim 16

MOS Transistors. Claim 16 is dependant on claim 2 and adds that the amplifying elements are MOS transistors. Sakamoto teaches a transistor. Sakamoto, figure 2, col. 2, lines

22 – 33. Nishioka teaches the use of field effect transistors (FET). Nishioka, col. 5, line 59 – col. 6, line 5. Fujii teaches MOS transistors. Fujii, figure 1; and col. 6, lines 12 – 14.

Sakamoto does not teach that the transistors are MOS transistors and Fujji uses the MOS transistors in a slightly different way in the circuit. Nishioka does not specifically use the term "MOS transistors."

The Electrical Engineering Handbook teaches the use of MOS transistors. Handbook, p. 567 – 580.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use MOS transistors for transistors in the data driver power circuit of Sakamoto. The Handbook teaches that MOS transistors allow easy fabrication using lithographic processes, resulting in integrated circuits (ICs), with very small devices, very large device counts, and very high reliability at low cost. MOS transistors also allow manufacture of complex systems without expensive packaging or cooling requirements. Handbook, p. 568. A MOS transistor, often labeled a MOS-FET, is a type of field effect transistor.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al., Fujii et al., and Suzuki et al., as applied to claim 1 above, and further in view of Ishizaki, et al., USPN 5,473,289.

Claim 13

Operational Amplifiers. Claim 13 is dependant on claim 1 and adds that the amplifying elements are operational amplifiers.

Sakamoto does not teach the use of operational amplifiers. Fujii teaches operational amplifiers but in a slightly different way than described in claim 13. Fujii, figure 1 and col. 6, lines 31 – 34.

Ishizaki, however, teaches the use of a temperature control circuit 101 having a operational amplifier with the control terminal connected to a plurality of diodes to ground and a resister to the voltage source. Ishizaki, figure 6(b), col. 7, lines 49 – 57.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the temperature control circuit of Ishizaki with the data driver power circuit of Sakamoto. Ishizaki teaches that such a circuit "generates a voltage which is proportion to the detected voltage." Ishizaki, col. 7, lines 29 – 30. See also Ishizaki, col. 8, lines 2 – 7; and figure 3. One would be motivated to use the Ishizaki circuit because operational amplifiers are readily available and the Ishizaki circuit has a linear output.

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al., Sakamoto et al., Suzuki et al., and Nishioka, et al. as applied to claim 2 above, and further in view of Ishizaki et al.

Claim 17

Operational Amplifiers. Claim 17 is dependant on claim 2 and adds that the amplifying elements are operational amplifiers.

Sakamoto and Nishioka do not teach the use of operational amplifiers. Fujii teaches operational amplifiers but in a slightly different way than described in claim 13. Fujii, figure 1 and col. 6, lines 31 – 34.

Ishizaki, however, teaches the use of a temperature control circuit 101 having a operational amplifier with the control terminal connected to a plurality of diodes to ground and a resister to the voltage source. Ishizaki, figure 6(b), col. 7, lines 49 – 57.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the temperature control circuit of Ishizaki with the data driver power circuit of Sakamoto. Ishizaki teaches that such a circuit "generates a voltage which is proportion to the detected voltage." Ishizaki, col. 7, lines 29 – 30. See also Ishizaki, col. 8, lines 2 – 7; and figure 3. One would be motivated to use the Ishizaki circuit because operational amplifiers are readily available and the Ishizaki circuit has a linear output.

Response to Arguments

12. Applicant's arguments filed July 29, 2002 have been fully considered but they are not persuasive.

Examiner rejected claim 1 under 35 U.S.C. 103(a) as being unpatentable over Fujii et al., in view of Sakamoto et al. In response, applicant amended claim 1 to add a capacitor between the output of the amplifying element and ground. Applicant argued that neither Fujii nor Sakamoto show a capacitor to ground at the output. Examiner rejects this argument because it would be obvious to place such a capacitor to ground high frequency noise.

Applicant argued that Sakamoto, in figures 2, 3, 7, and 8, only teaches two diode in series. Examiner rejects such argument both because applicant's use of the word plurality in claim 1 would include two or more diodes and because Sakamoto, in figure 1 and in col. 2, line 22 – col. 3, line 26, shows that the number of diodes is not limited to two or less.

As to claims 2 – 17, applicant argues that these claims are allowable as dependant on claim 1. Examiner's prior rejections of claims 2 – 17 are otherwise unrebutted.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bizen, USPN 5,379,003, describes a capacitor at an emitter to ground high frequency noise.

Morozumi, USPN 4,582,395, teaches a capacitor 19 at the output of a transistor to store a charge to a LCD element. Morozumi, figure 3a.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600